REMARKS

This paper is being provided in response to the Office Action mailed May 6, 2005, for the above-referenced application. In this response, Applicant has amended claims 1, 2, 13, 14, 15, 18 and 19 to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification.

Applicant thanks the Examiner for the indication of allowable subject matter in claims 2-12 and 15-17. Applicant has rewritten claims 2 and 15 into independent form to incorporate the features of the base claim and any intervening claims. The remaining claims depend therefrom. Applicant has addressed below the rejections under 35 U.S.C. 112, second paragraph. Accordingly, Applicant respectfully submits that these claims are in condition for allowance.

The objection to the claims for informalities has been addressed by amendments to the claims contained herein. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claim 1, and its dependent claims, and claims 14-17 under 35 U.S.C. 112, second paragraph, as lacking support in the specification has been addressed by amendments to the claims herein. Applicants have amended the claims to recite that the switching unit connects the first charge pump circuit, the second charge pump circuit and a first node in series in response to a first switching signal and a control signal. Applicant directs attention, for example, to page 23, lines 7-20 of the present specification and the features as

illustrated in FIG. 5. Accordingly, Applicant respectfully submits that this rejection should be reconsidered and withdrawn.

The rejection of claims 13 and 18 under 35 U.S.C. 112, second paragraph, as being indefinite has been addressed by amendments to the claim contained herein. Applicant has amended claim 13 to clarify that a switching unit connects a first group of J charge pump circuits in series and connects a second group of K charge pump circuits in series, wherein J and K are integers greater than 2 and less than N (the total number of charge pump circuits). Applicant respectfully submits that the claim, as presently recited, is clear and definite and would be readily understood by one of ordinary skill in the art. Further, Applicant refers to the discussion above with respect to the 112, second paragraph, rejection of claim 1 and the further amendments made herein. Accordingly, Applicant respectfully submits that this rejection should be reconsidered and withdrawn.

The rejection of claims 1, 13, 14 and 18-20 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,801,577 to Tailliet (hereinafter "Tailliet") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 1, as amended herein, recites a boosting circuit including first, second and third charge pump circuits containing first, second and third capacitive sections all charged to a first voltage. A switching unit connects the first charge pump circuit, the second charge pump circuit and a first node in series in response to a first switch signal and a control signal

such that a second voltage higher than said first voltage is outputted from the first node to a first internal circuit of a semiconductor device. The switching unit further connects the first charge pump circuit, the second charge pump circuit, the third charge pump circuit and a second node in series in response to a second switch signal and the control signal, such that a third voltage is outputted from the second node to a second internal circuit of the semiconductor device.

Independent claim 13, as amended herein, recites a boosting circuit including N charge pump circuits to which a power supply voltage is supplied, wherein N is an integer of two or more. A switching unit connects a first group of J charge pump circuits among the N charge pump circuits and a first node in series in response to a control signal and first switching signal, wherein J is an integer satisfying $2 \leq J \leq N$, to output a voltage equal to J + 1 times the power supply voltage from the first node to a first internal circuit of a semiconductor device. The switching unit further connects a second group of K charge pump circuits among the N charge pump circuits and a second node in series in response to the control signal and a second switching signal, wherein K is an integer satisfying $2 \leq K \leq N$, to output a voltage equal to K+1 times the power supply voltage from the second node to a second internal circuit of the semiconductor device.

Independent claim 14, as amended herein, recites a semiconductor device including a boosting circuit and first and second internal circuits connected to the boosting circuit via first and second nodes. The boosting circuit includes first, second and third charge pump circuits containing first, second and third capacitive sections all charged to a first voltage. A switching unit connects the first charge pump circuit, the second charge pump circuit and the first node in

series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from the first node to the first internal circuit of a semiconductor device. The switching unit further connects the first charge pump circuit, the second charge pump circuit, the third charge pump circuit and the second node in series in response to a second switch signal and the control signal, such that a third voltage is outputted from the second node to the second internal circuit of the semiconductor device.

Independent claim 18, as amended herein, recites a semiconductor device including a boosting circuit and first and second internal circuits connected to the boosting circuit via first and second nodes. The boosting circuit includes N charge pump circuits to which a power supply voltage is supplied, wherein N is an integer of two or more. A switching unit connects a first group of J charge pump circuits among the N charge pump circuits and the first node in series in response to a control signal and first switching signal, wherein J is an integer satisfying $2 \leq J \leq N$, to output a voltage equal to J + 1 times the power supply voltage from the first node to the first internal circuit of a semiconductor device. The switching unit further connects a second group of K charge pump circuits among the N charge pump circuits and the second node in series in response to the control signal and a second switching signal, wherein K is an integer satisfying $2 \leq K \leq N$, to output a voltage equal to K+1 times the power supply voltage from the second node to the second internal circuit of the semiconductor device.

Independent claim 19, as amended herein, recites a method of boosting a voltage. First and second capacitors are charged to a first voltage in first and second modes. A potential of the first capacitor is boosted to twice that of the first voltage in said first and second modes. The

first and second capacitors are connected in series in the first mode to output a second voltage. A third capacitor is charged to the first voltage in the second mode. The first, second and third capacitors are connected in series in the second mode to output a third voltage. The method includes switching between first and second modes in response to a control signal and first and second switch signals. Claim 20 depends from independent claim 19.

The Tailliet reference discloses a high voltage generator including a circuit with a network of capacitors and switching transistors having two modes of functioning. The first mode isolates all the capacitors and simultaneously charges them to the level of the supply voltage. The second mode connects all the capacitors in series between the supply voltage and an output node of the network in order to instantaneously increase the voltage level of this output node to a voltage level that is greater than the supply voltage. (See Abstract and col. 2, line 63 to col. 3, line 8 of Tailliet.) The Office Action references specifically Figure 7 of Tailliet.

Applicant's independent claims, as amended herein, recite a boosting circuit and a method for boosting a voltage that includes at least the features of charge pump circuits charged to a first voltage and a switching unit that connects one group of charge pump circuits and a first node in response to a control signal and a first switching signal to output a second voltage from the first node, and connects a second group of charge pump circuits and a second node in response to the control signal and a second switch signal to output a third voltage from the second node. Applicant has found that a boosting circuit and method according to the presently claimed invention provides for a reduced circuit area that more efficiently provides desired boosting functionality. (See, for example, page 24, lines 10-26 of the present specification.)

Applicant respectfully submits that Tailliet does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Specifically, as seen in Figure 7 of Tailliet, cited in the Office Action, Tailliet discloses a circuit having a network of capacitors that are all connected in series between a supply voltage and one output node (mout). As discussed above, Tailliet's first mode isolates the capacitors to charge them and the second mode connects all these capacitors between the supply voltage and the output node in order to instantaneously increase the voltage level of the output node. In contrast, Applicant discloses boosting circuit including a switching unit that is responsive to a control signal and first and second switching signals and which utilizes combinations of charge pump circuits to efficiently output different voltages from at least two nodes of the circuit to first and second internal circuits of a semiconductor device.

Accordingly, Applicant respectfully submits that the prior are does not disclose a boosting circuit and a method for boosting a voltage that includes at least the features of charge pump circuits charged to a first voltage and a switching unit that connects one group of charge pump circuits and a first node in response to a control signal and a first switching signal to output a second voltage from the first node, and connects a second group of charge pump circuits and a second node in response to the control signal and a second switch signal to output a third voltage from the second node, as is claimed by Applicant. In view of the above, Applicant respectfully request that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART LLP

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Donald W. Muirhead
Registration No. 33,978

Customer No.: 26339

Choate, Hall & Stewart LLP
Exchange Place
53 State Street
Boston, MA 02109
Phone: (617) 248-5000
Fax: (617) 248-4000